

The diagram illustrates a memory chip layout. At the bottom, a large rectangular area is labeled 'LOGIC REGION'. Above it, a smaller rectangular area is labeled '32 DRAM REGION'. A bracket on the left side of the diagram groups both the logic region and the DRAM region, with the label 'FIG. 1' positioned above the bracket.

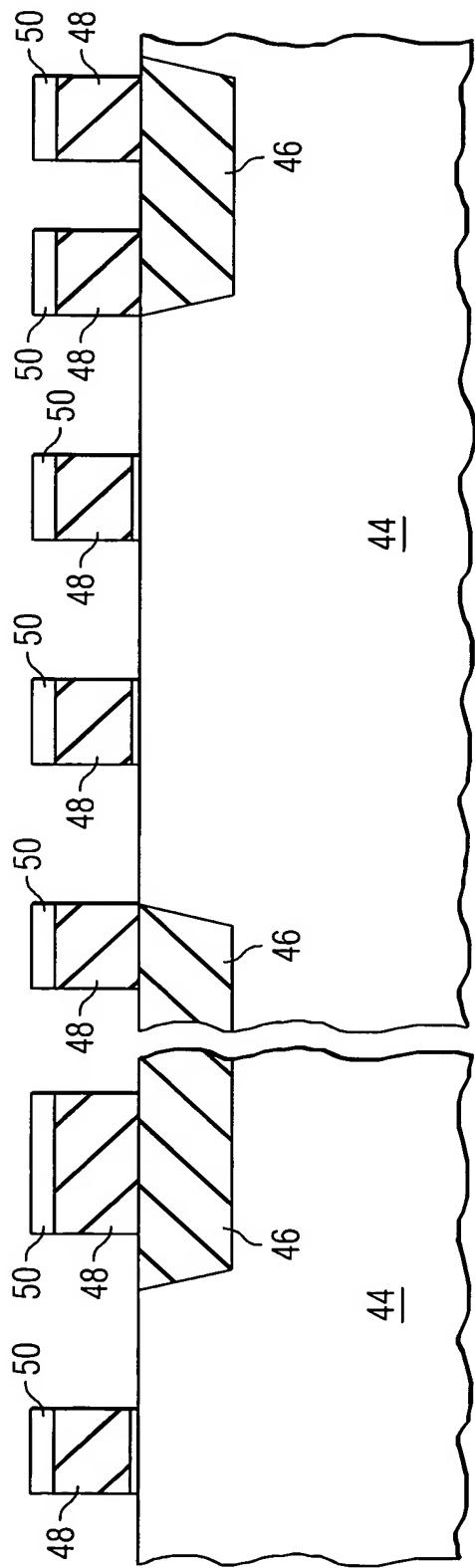
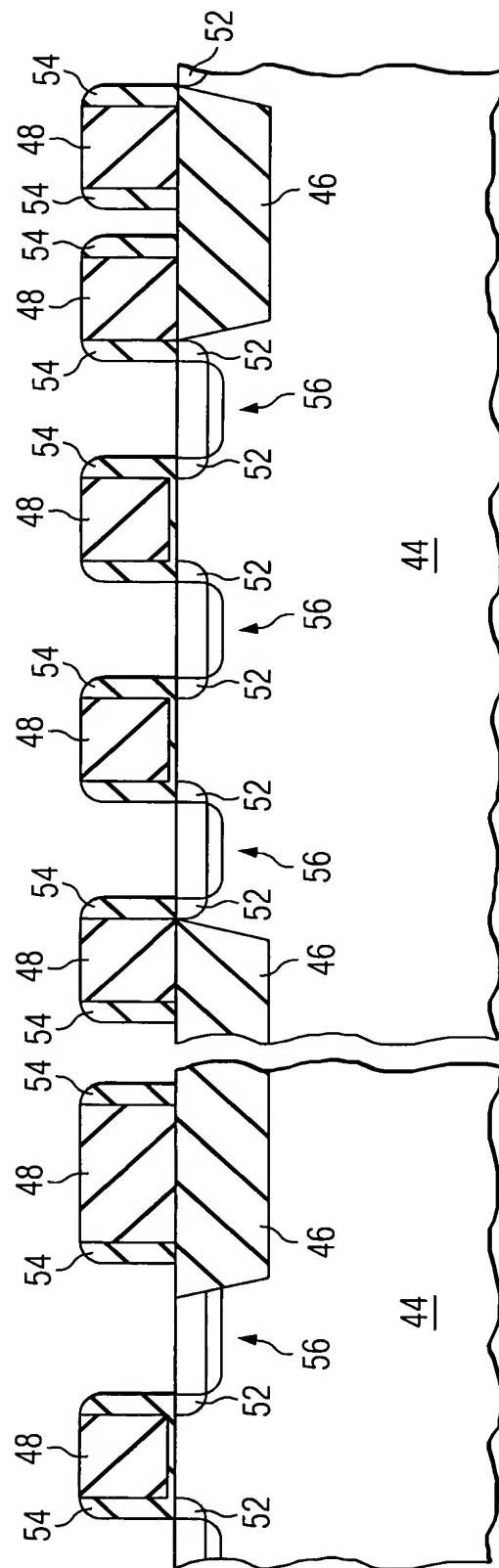


FIG. 2

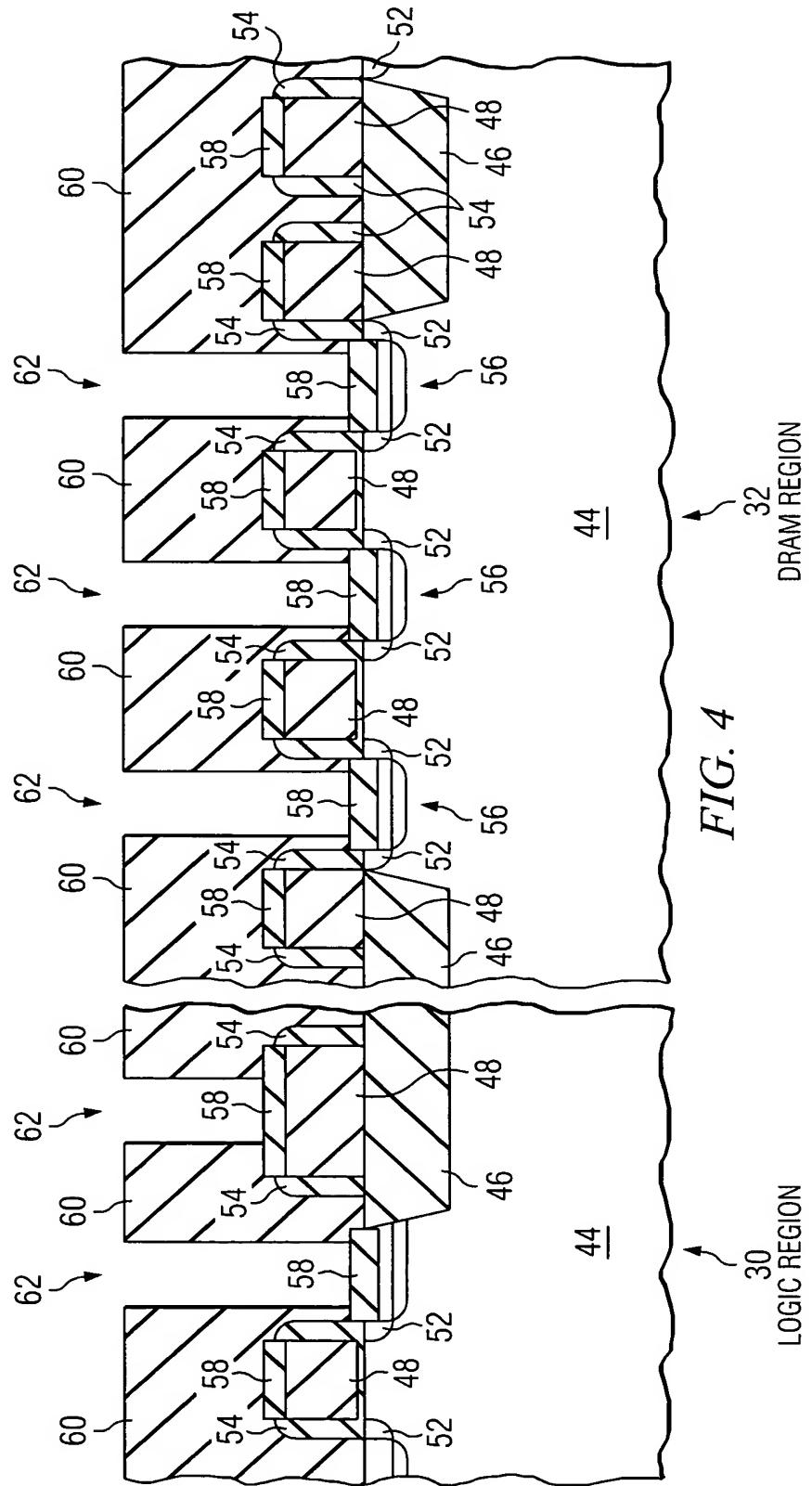
30 LOGIC REGION

32 DRAM REGION

The diagram illustrates a memory structure. At the bottom, a bracket labeled '30 LOGIC REGION' spans the width of the structure. Above it, a bracket labeled '32 DRAM REGION' spans the width of the structure. The '32 DRAM REGION' is positioned above the '30 LOGIC REGION'.



*FIG. 3*  A diagram showing a rectangular array of memory cells. The array is divided into two main regions: a "LOGIC REGION" on the left and a "DRAM REGION" on the right. The DRAM REGION is further subdivided into four quadrants, with the top-right quadrant specifically labeled "32 DRAM REGION". A curved arrow points from the text "32 DRAM REGION" to this quadrant. The text "FIG. 3" is centered above the array.



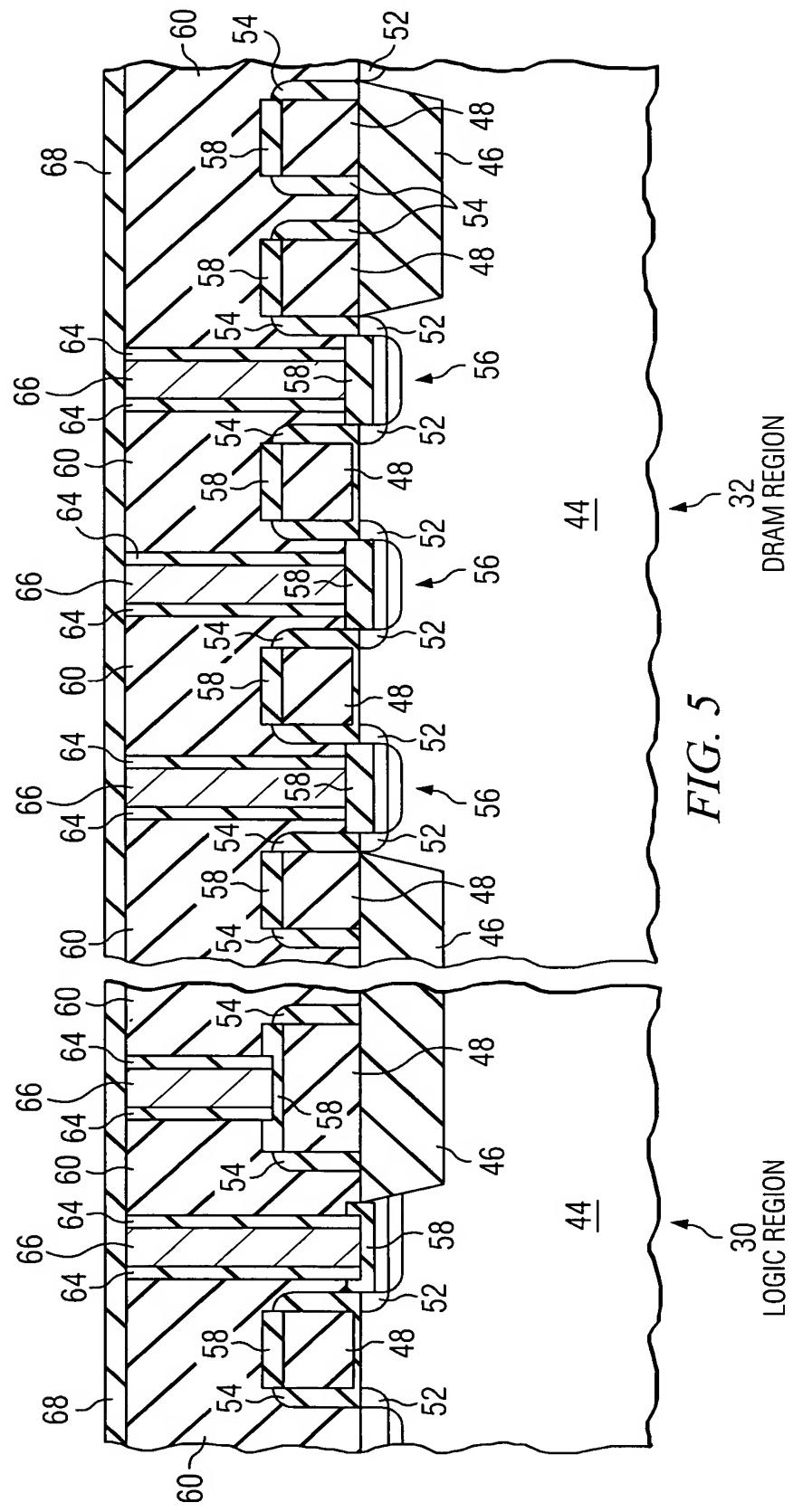


FIG. 5

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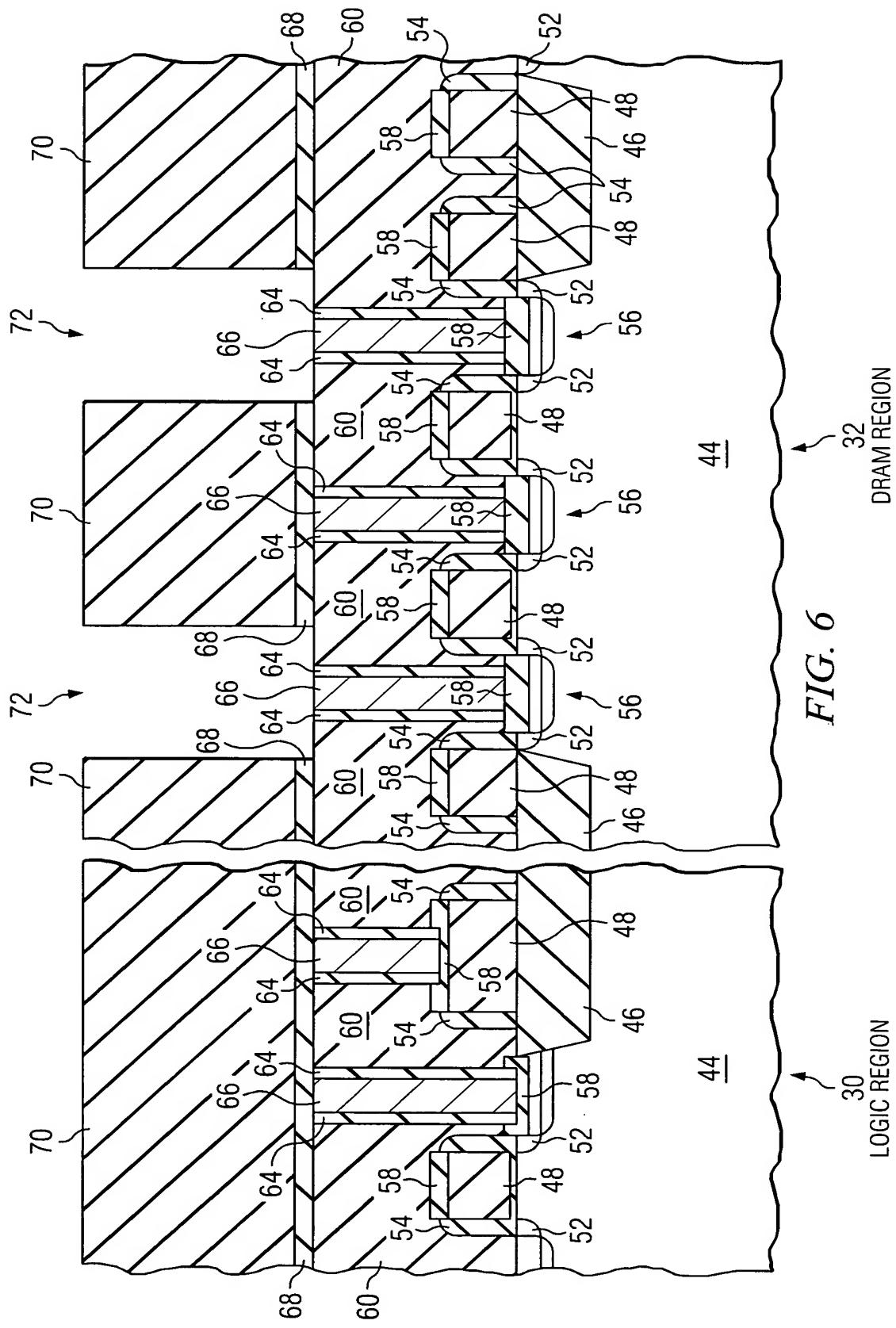
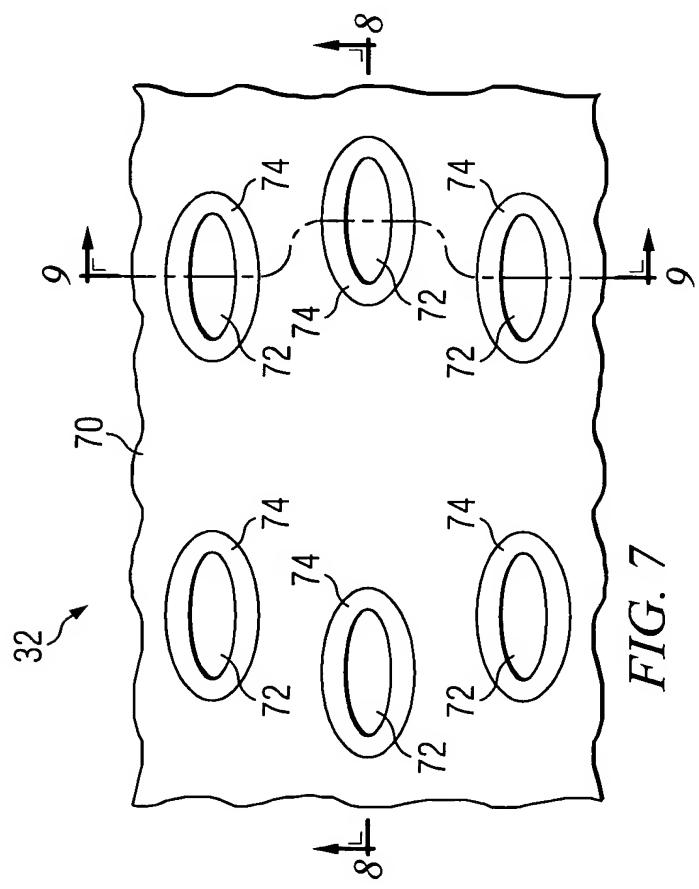
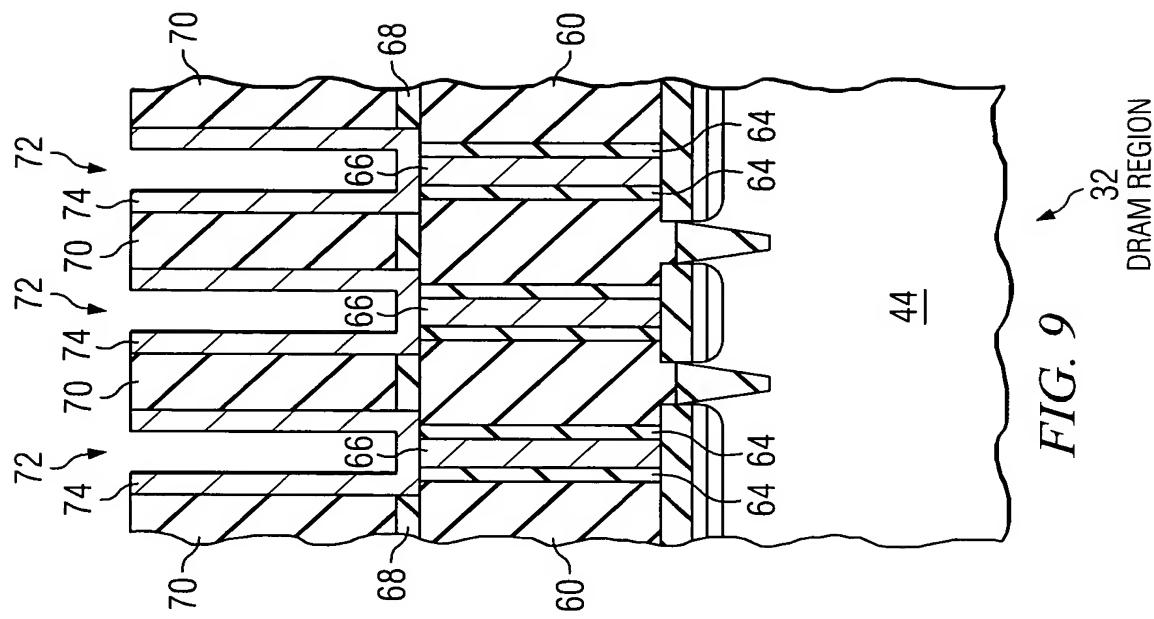
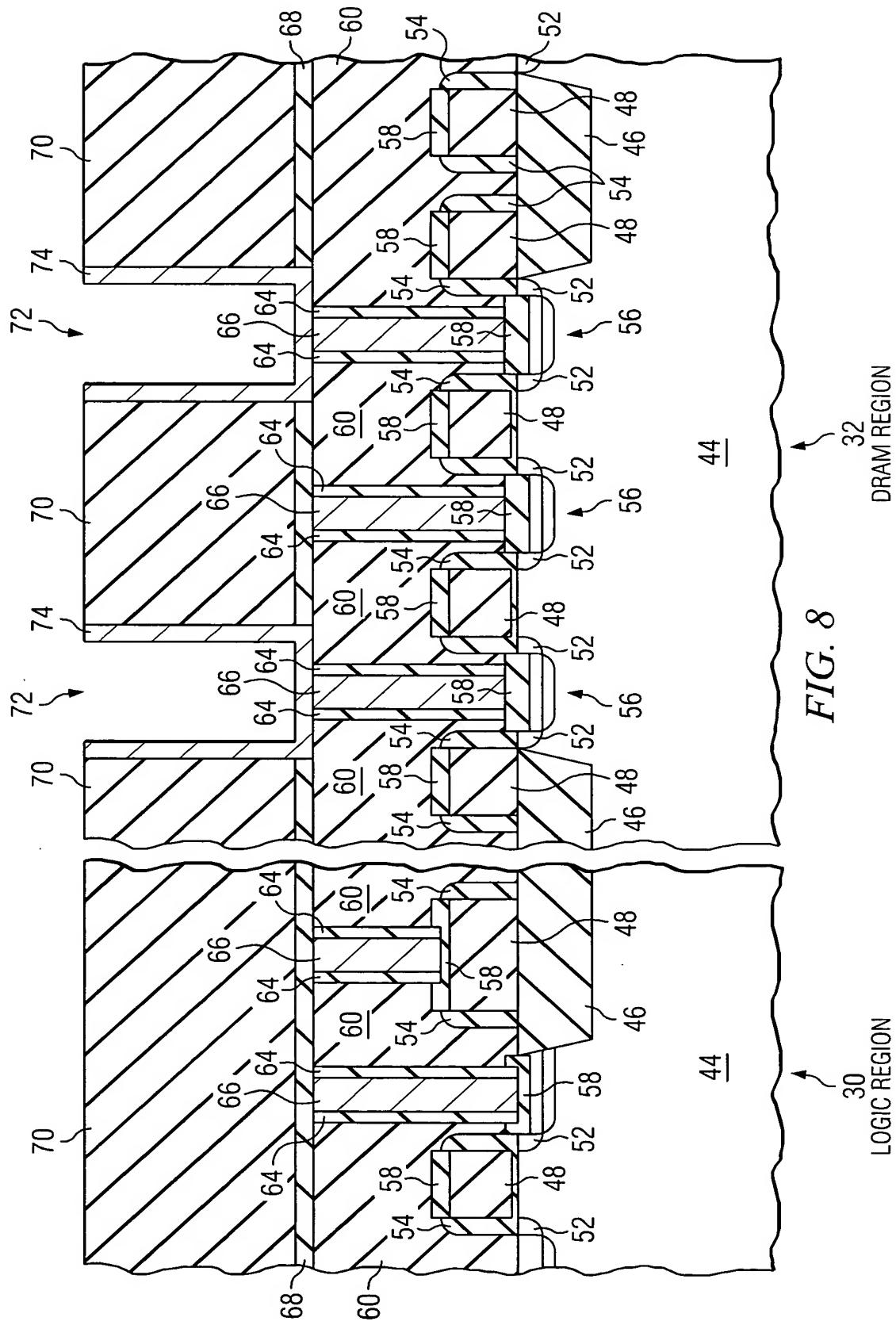


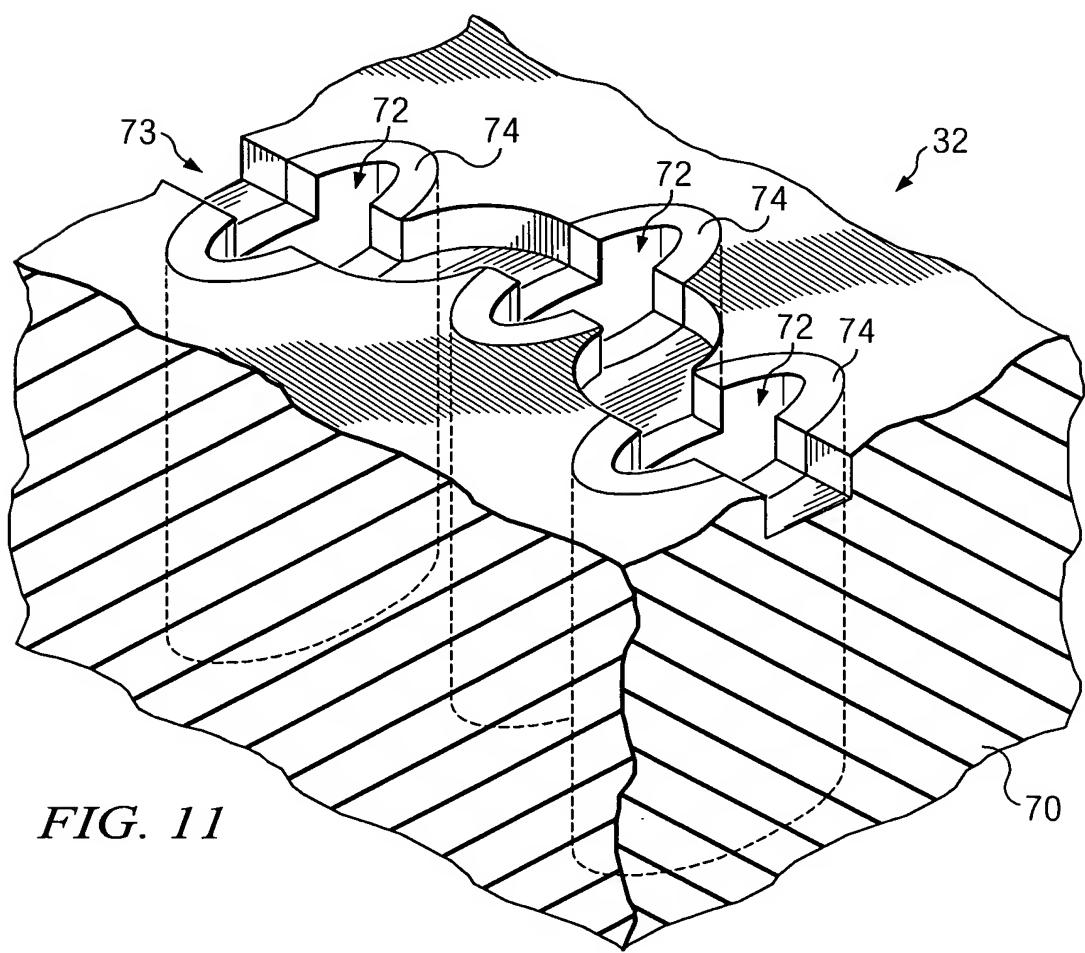
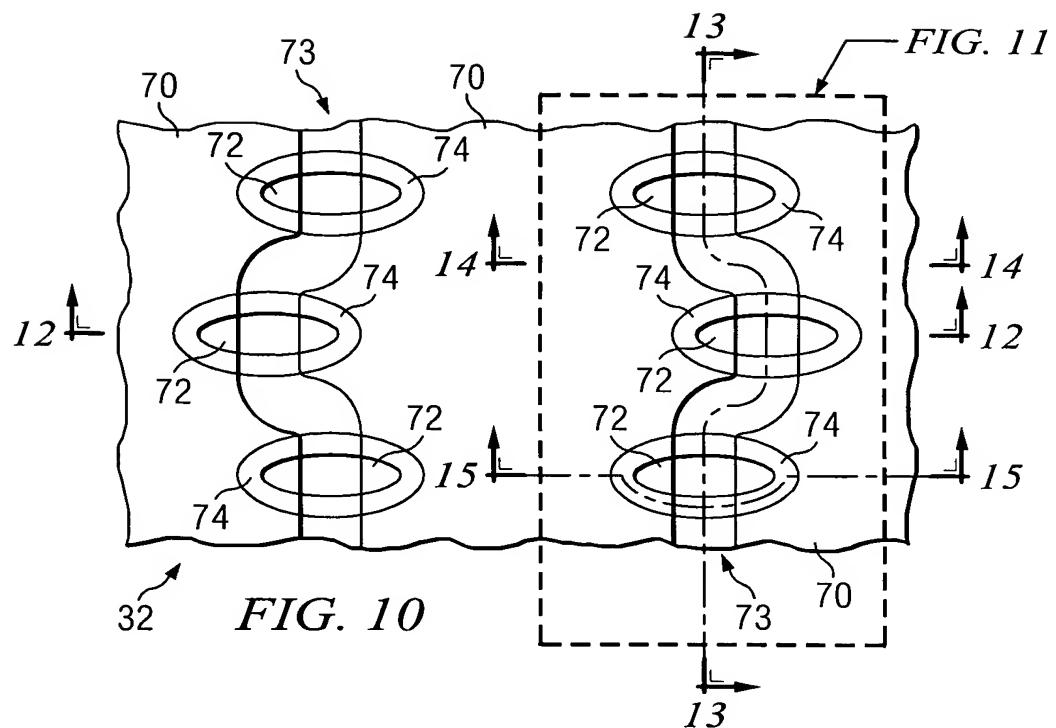
FIG. 6



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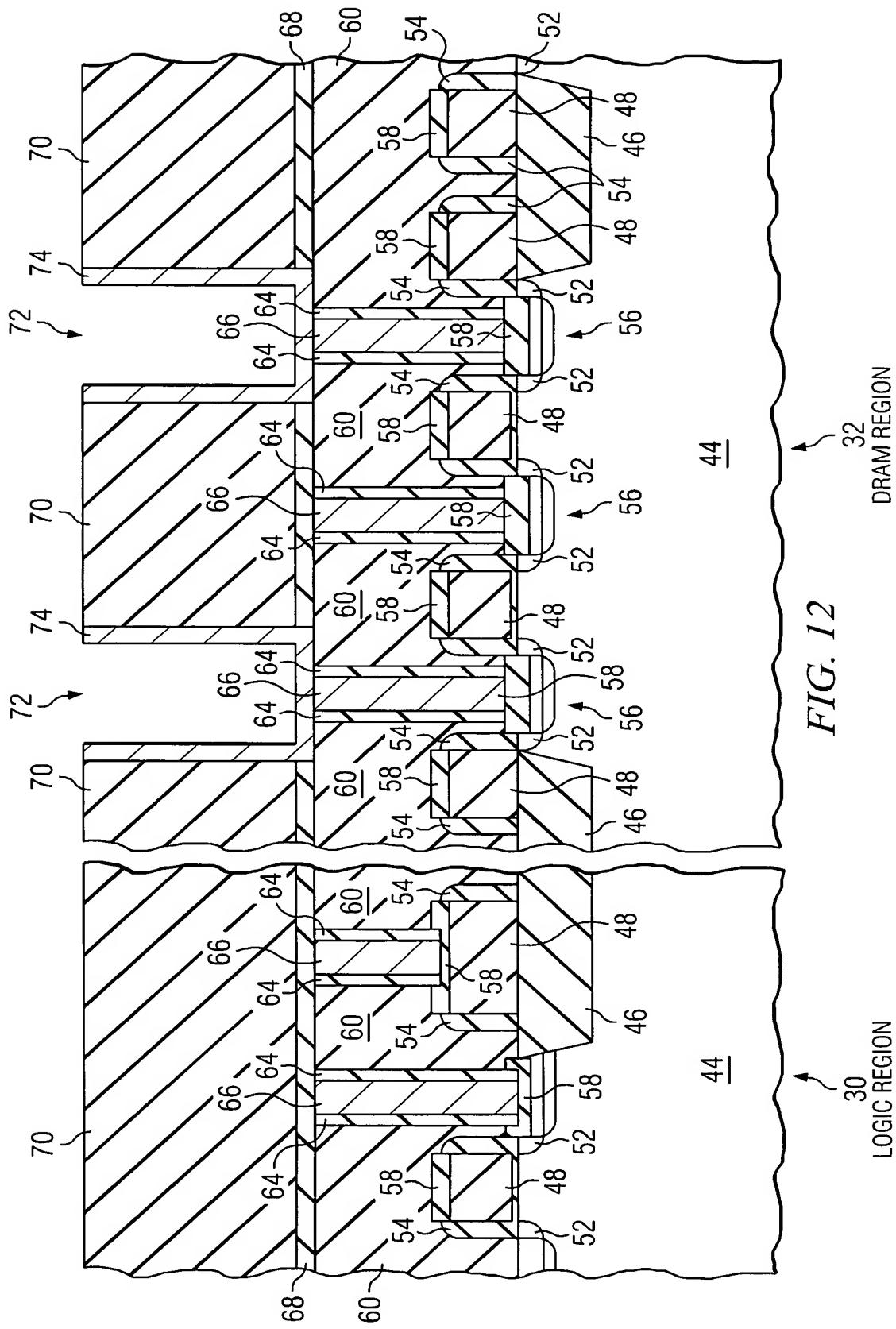


FIG. 12

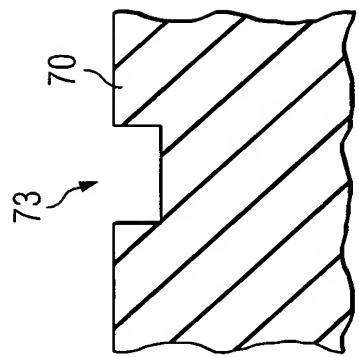


FIG. 14

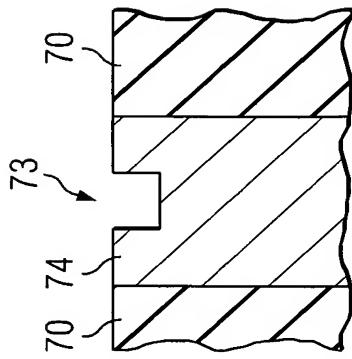


FIG. 15

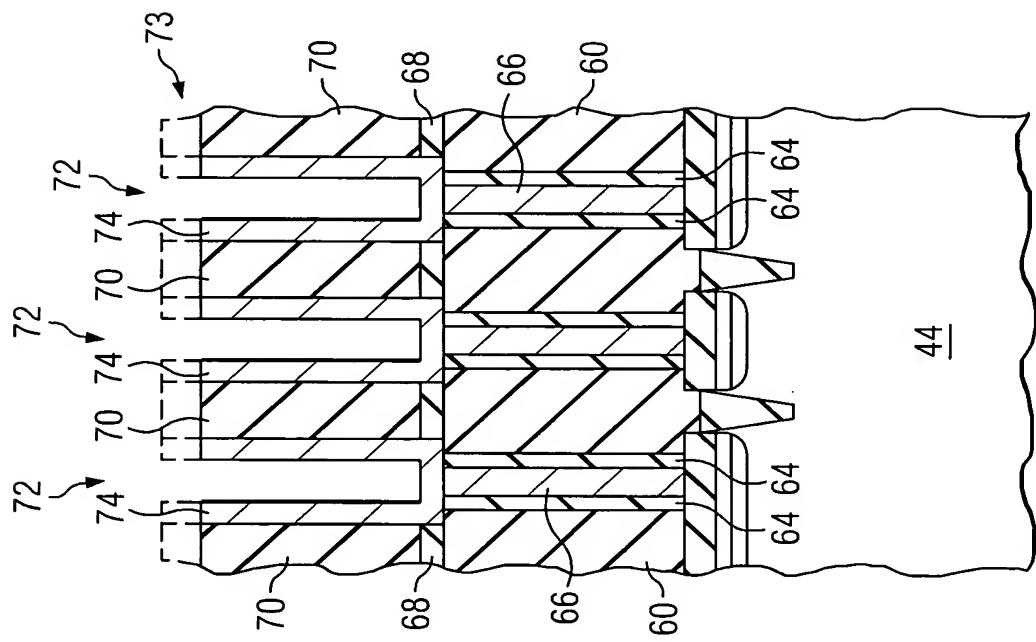
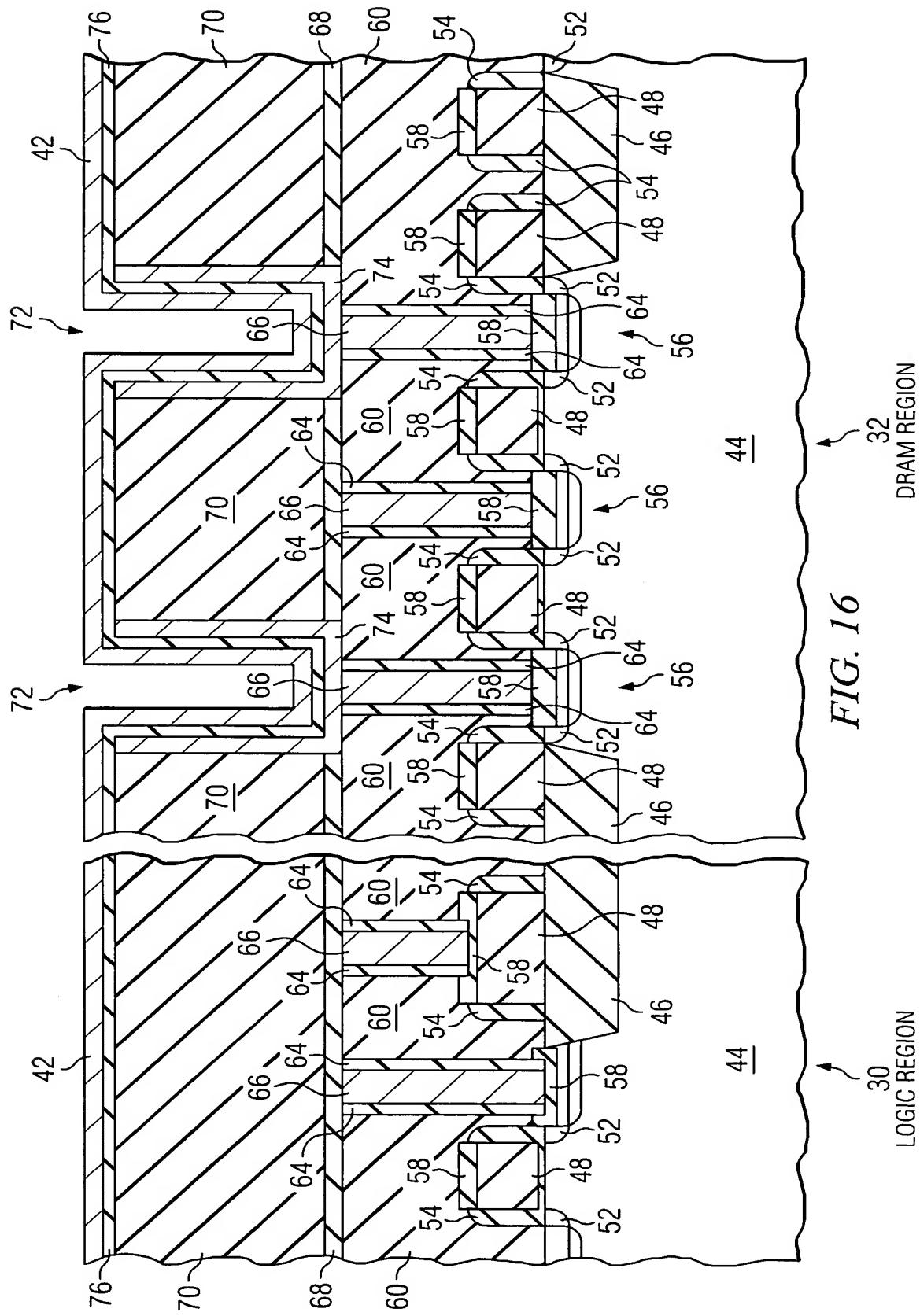
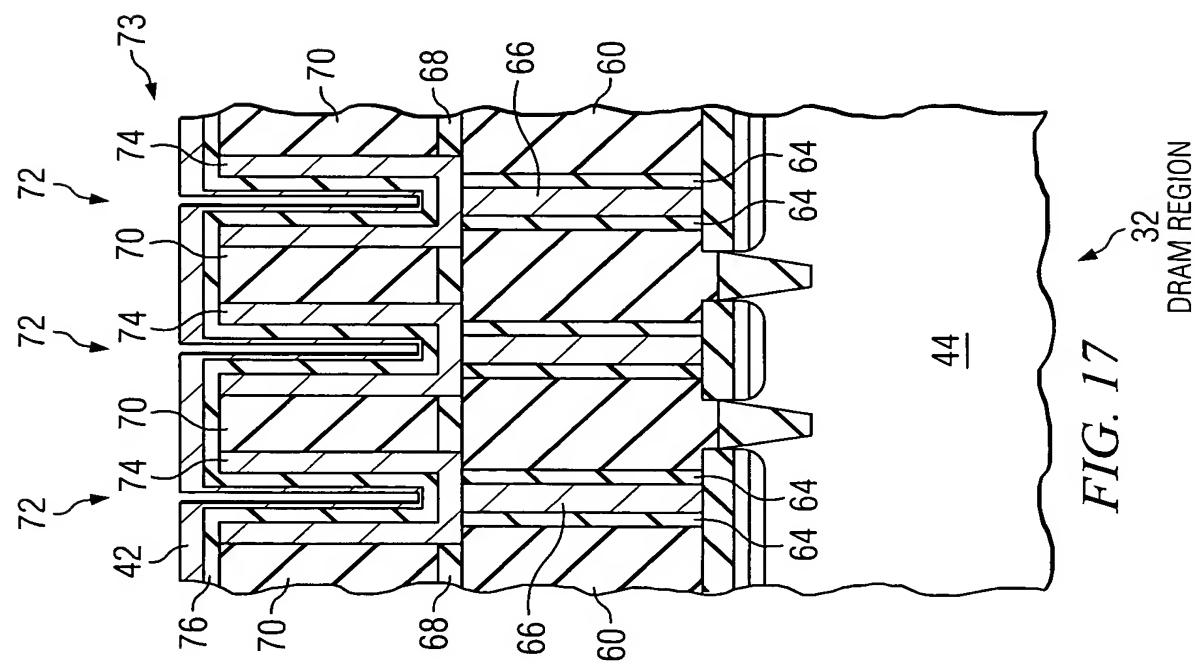
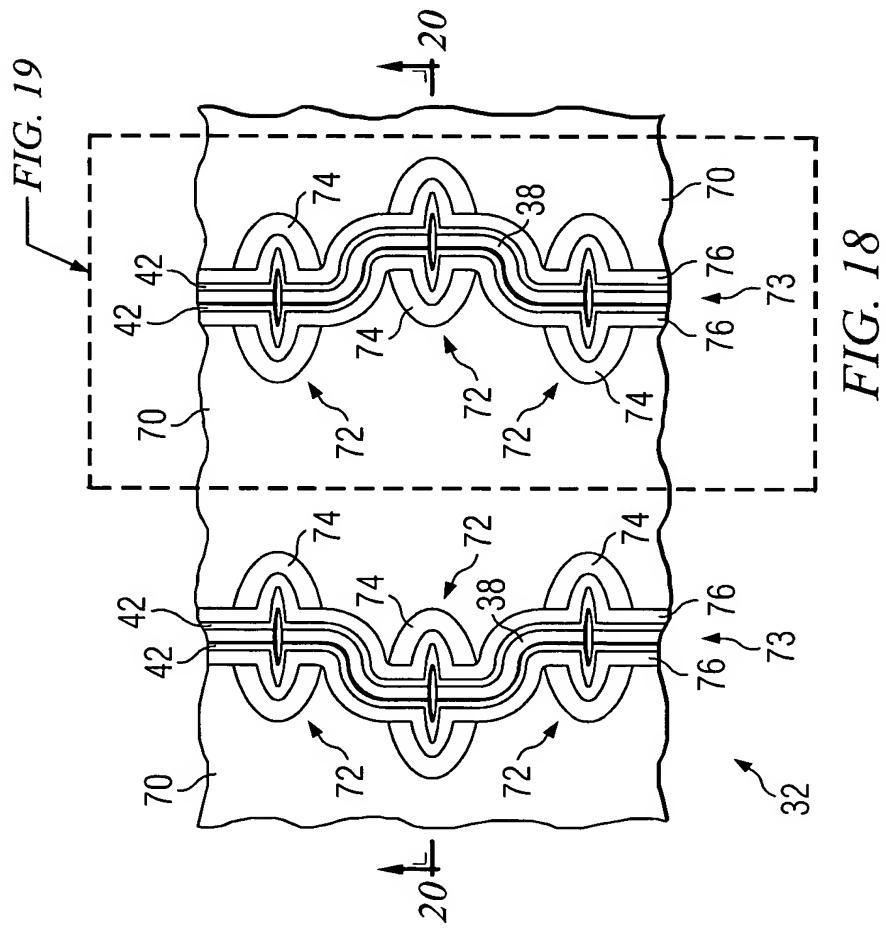


FIG. 13 32 DRAM REGION

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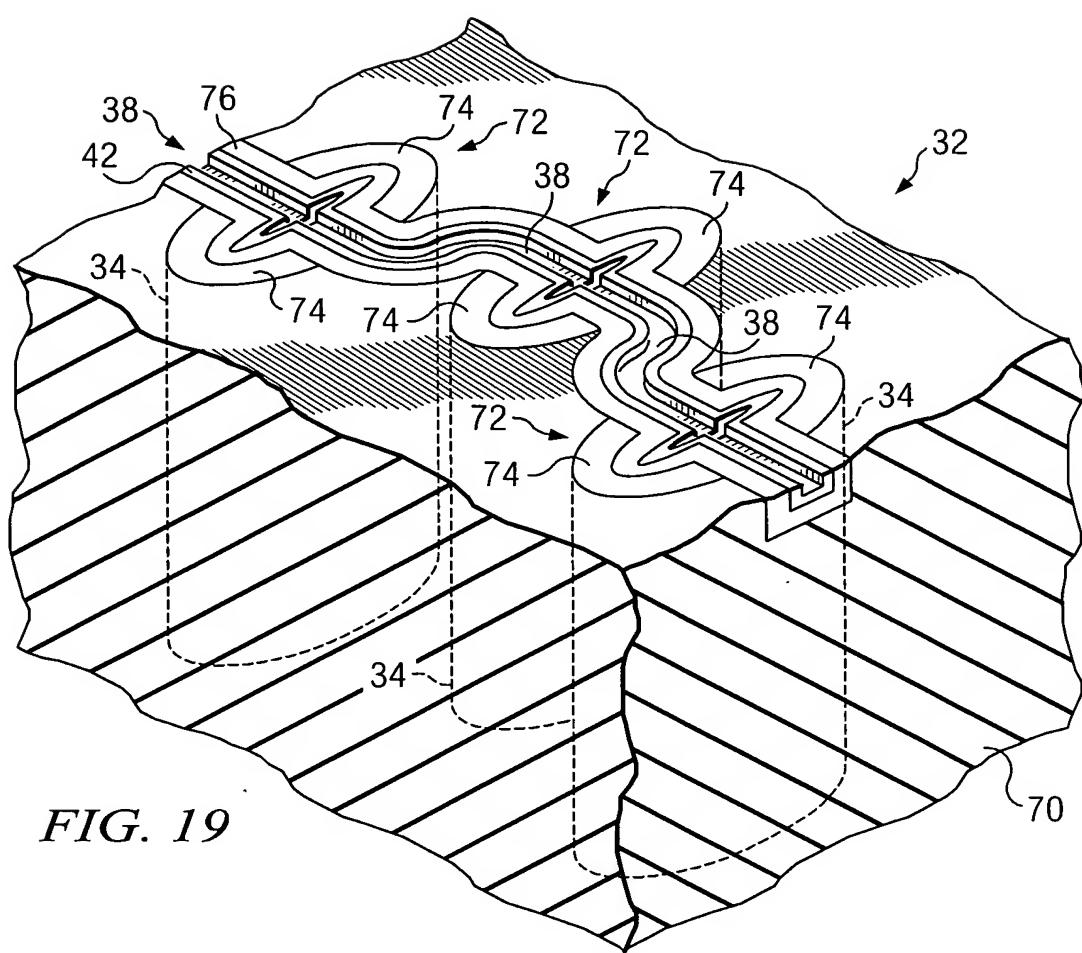


FIG. 19

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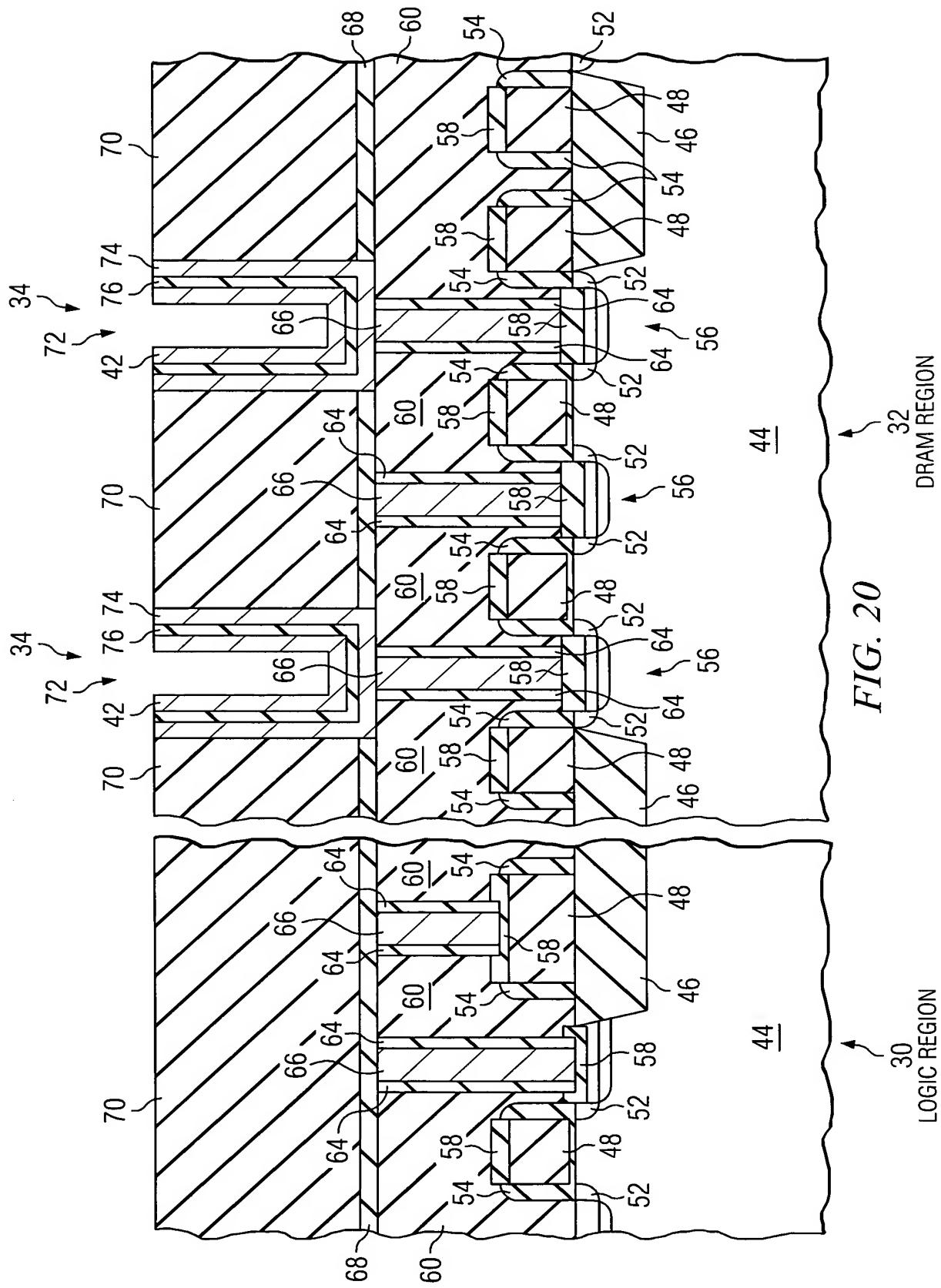
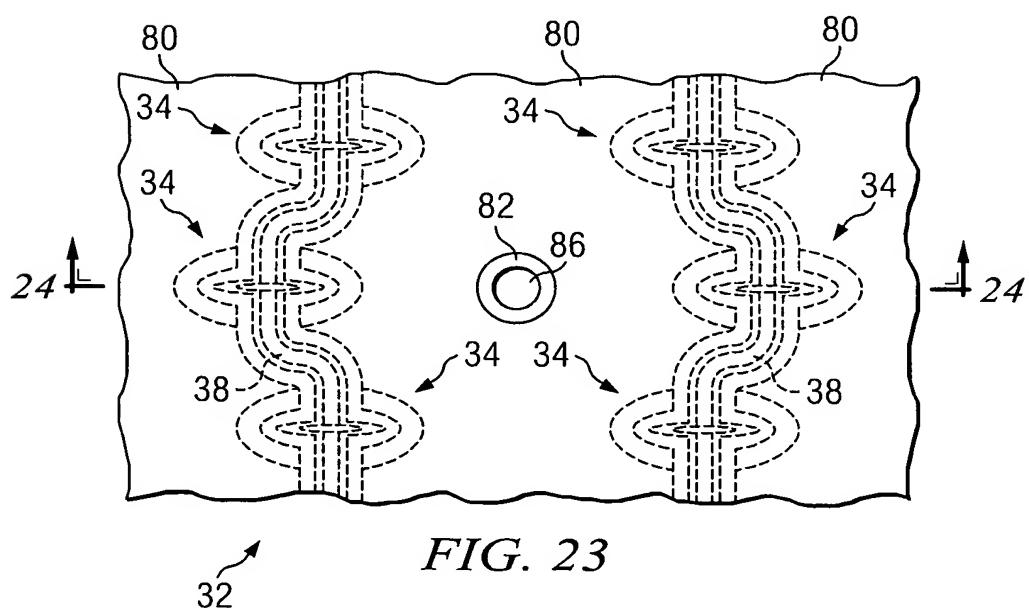
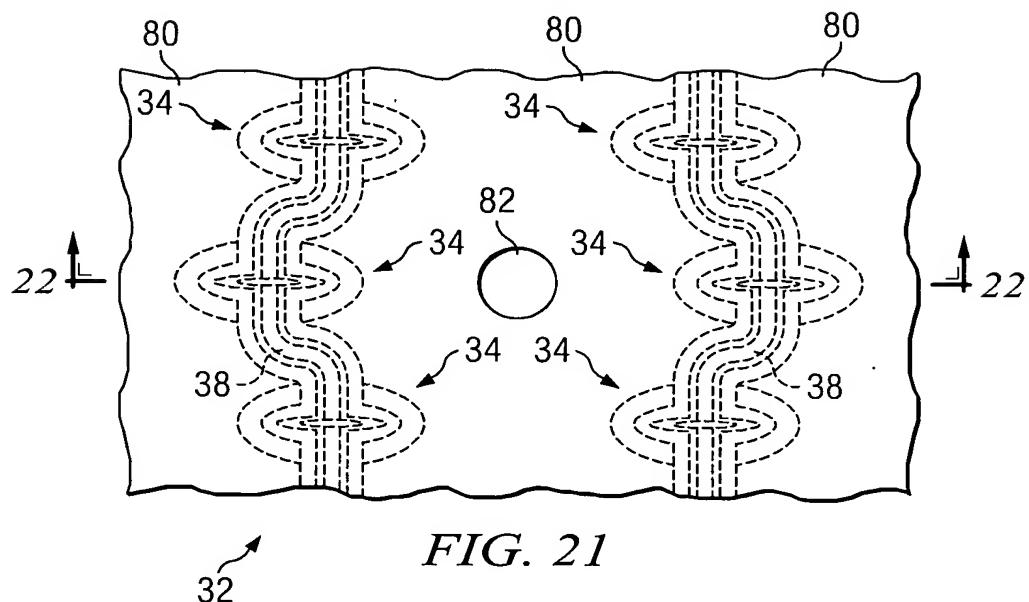


FIG. 20



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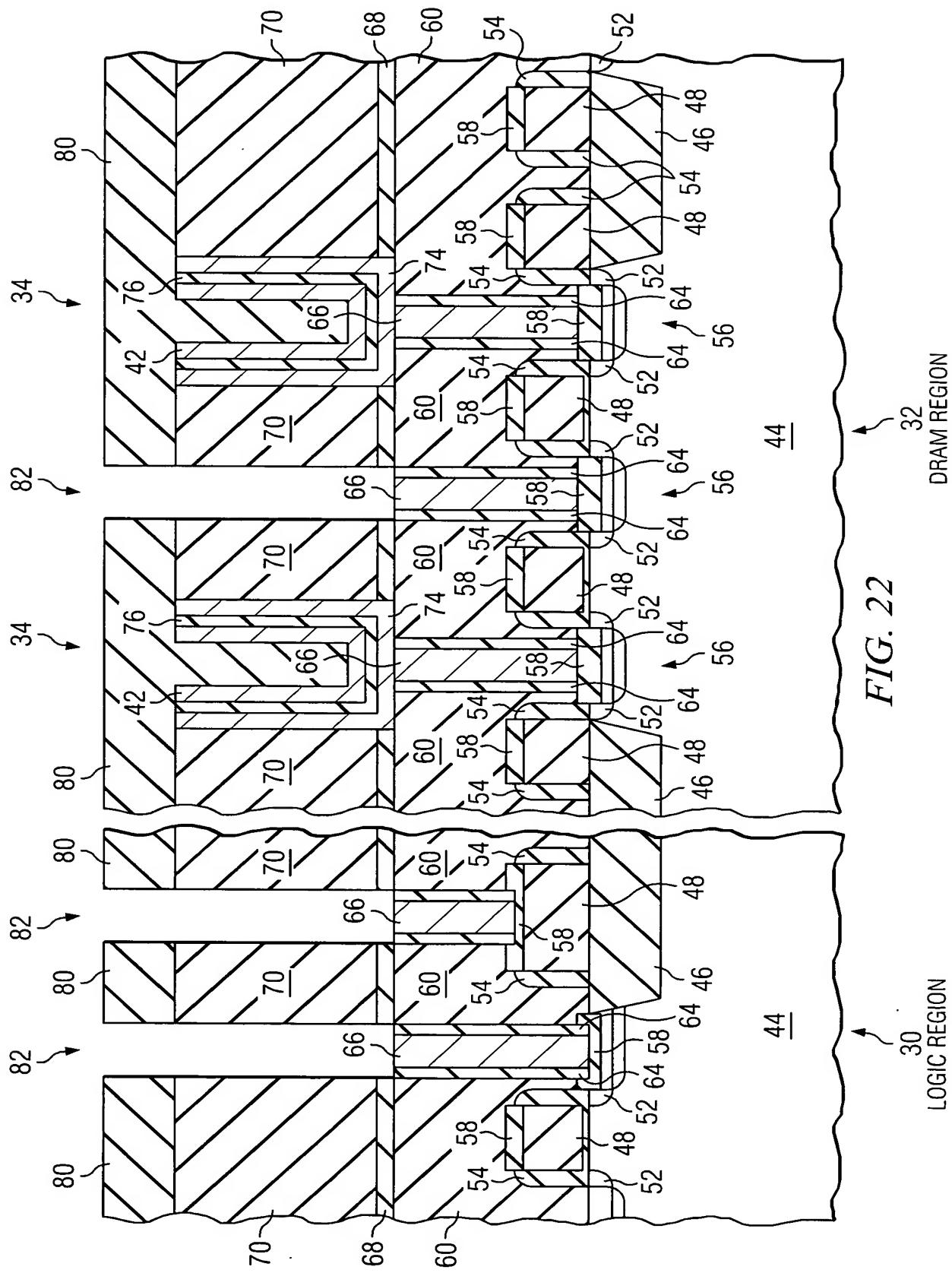


FIG. 22

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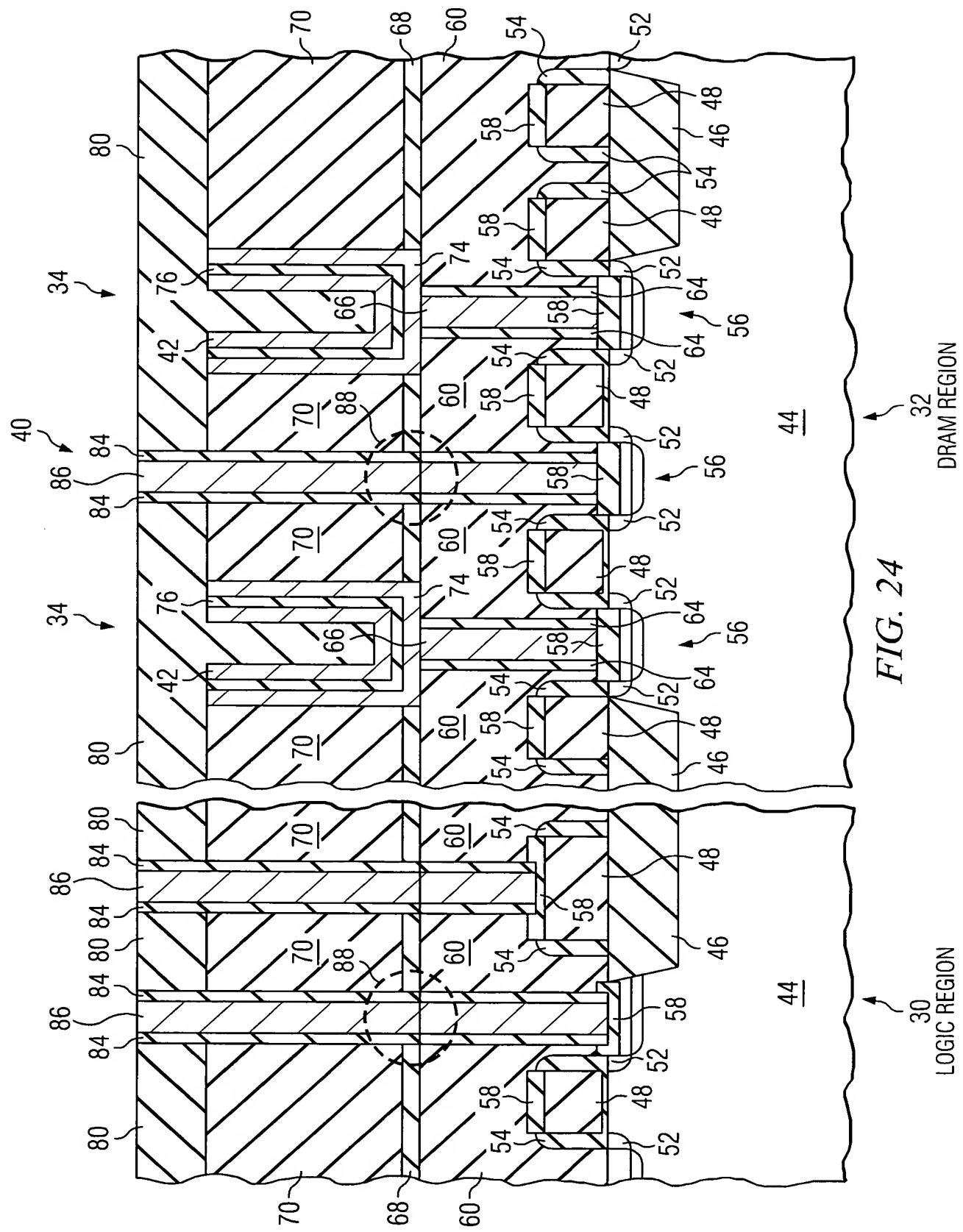


FIG. 24